8 BITS NAND CPU 8.2.0 REFERENCE DATA

8 bits data bus and 12 bits address bus

7 8 bits general purpose registers (r0=constant)

4 16 bits double registers Global Pointer, Stack Pointer, Return Address and Accumulator

Interrupts at end of current instruction

Memory mapped I/O for keyboard and a 16 char hex led screen with GPU

CORE INSTRUCTION SET

MOVE 0YX0 Y=X REGISTERS

ADD (c) 1YXZ y=X+Z 0 Cost 1

ADD (c) 1YXZ Y=X+Z 2 3

4 5

INC (c) 20YX Y=X+1 6 Load Store 7 Mem Index

NOT 21YX Y=NOT(X) 8-9 GP Global Pointer

SLL (c) 22YX Y=SLL(X) A-B SP Stack Pointer

XOR 23YX Y=XOR(Y,X) C-D RA Return Address

SRL (c) 24YX Y=SRL(X) E-F Acc Kernel Reserved

SUB 25YX Y=Y-X

Multi 26YX HiLo=Y\*X

Div 27YX Hi=Reminder Lo=Y/X

Read Hi 28Y0 Y=Hi

Read Lo 29Y0 Y=Lo

Read C out 2AY0 Y=Carry out

Read Sign 2BY0 Y=Sign(X)

LOAD r/r 4YXZ Y=MEM(rX+rZ) 4YA0 Y=MEM(SP)

STORE r/r 5YXZ MEM(rX+rZ)=Y 4Y81 Y=MEM(GP+r1)

LOAD a/r 6adr r6=MEM(adr+r7)

STORE a/r 7adr MEM(adr+r7)=r6

LOAD Imm 8Yxx Y=xx

LOAD 9adr r6=MEM((adr)

STORE Aadr MEM(adr)=r6

GOTO Badr PC=adr

CALL Cadr PC=adr RA=PC

BRANCH 0 Dadr IF r6=0 PC=adr

BRANCH C.out Eadr If C.out=1 PC=adr

POP F0Y0 MEM(SP)=Y + SP=SP-1

PULL F1Y0 SP=SP+1 + Y=MEM(SP)

TRAP FExx Int Flag=3 Int Reg

RETURN FFFE PC=RA

HALT FFFF Halt